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A REVIEW APPROACH OF POWER GRID ANALYSIS IN VLSI DESIGNS

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Abstract- One of the most critical challenges in today’s CMOS VLSI design is the lack of predictability in chip performance at design stage. One of the process variability comes from the voltage drop variations in on-chip power distribution networks. Power distribution systems in integrated circuits are used to provide the voltages and currents the devices need to operate properly. It provides the voltages and currents that devices in a circuit need to operate properly and silicon success requires its careful design and verification. In our work, we have Proposed the cell characterization methodology for instantaneous IR drop analysis as well as Power Up analysis for MTCMOS, computed resistances and capacitors based on technology data for 130nm node. A sample program was written to realize the mesh structure. This new algorithm is very efficient and scalable for huge networks with a large number of variation variables.

Keywords: Power grid, Verification, Simulation, Voltage drop

I. INTRODUCTION

The power distribution system design is an area of increasing concern in semiconductor industry. According to data in [1], more than 50% of tape outs using 0.13-micron technology would fail, if the power distribution system were not validated beforehand. Lower operating voltages, increased device integration density and leakage currents, higher operating frequencies and the use of low power design techniques; they all tend to stress the power grid as technology evolves. The design of such systems is complex and error-prone, since there is a wide variety of an aspect that must be taken into account. Of these, perhaps the four major problems that may affect power distribution systems are voltage drop, ground bounce, and L di/dt noise and electro migration [4].

Voltage drop, also called IR drop, is the voltage reduction that occurs on power supply networks. The IR drop can be static or dynamic and results from the existence of non-ideal elements: the resistance within the power and ground supply wiring and the capacitance between them. While static voltage drop considers only the average currents, dynamic voltage drop considers current waveforms within clock cycles and has a RC transient behavior. Similar effects may be found in ground wiring, usually referred as ground bounce. Both effects contribute to lower operating voltages within devices (i.e. logic cells/gates in digital circuits), which in general increase the overall time response of a device and might cause a failure in its operation. The L di/dt noise is caused by current spikes on wires that will induce abrupt voltage changes on these wires and their neighboring wires, due to inductance coupling [6], [2].

Power grid analysis and verification is, one of the most important steps in the design flow, yet computationally a very complex one. Power grid verification is usually accomplished by simulation [5], [9]. The disadvantage of simulation is that stimuli must be generated very carefully such that the relevant scenarios are accounted for. Only settings corresponding to the chosen stimuli are simulated and thus verified, so they should be chosen appropriately and should be representative of relevant situations. Since the power grid encompasses the whole die area, its description is rather large and the simulation process is slow and highly complex. These results from the necessity to take into account a huge number of power grid parameters (RLC non-idealities) and all the devices that take current from it, as shown in Fig. 1. Simulating the power grid with all the devices might be impossible for VLSI circuits, as it would consume too many resources. Furthermore, simulating for all possible device settings is also impossible, as it would take too long. In addition, given the size of current designs, it is also impossible to assume that designer intervention will be sufficient to generate appropriate sets of stimuli for the grid verification. Typically no single designer knows enough of the circuit behavior, as a whole, to perform such task. Even if that were possible, it would require considerable effort from designers and might delay significantly the design process. Therefore, an automatic way of generating realistic sets of stimuli given the knowledge of the actual circuit implementation is necessary.
A Review Approach Of Power Analysis In VLSI Designs

Figure 1. A Simplified power grid model.

Hopefully, this task can be integrated in a standard design & verification framework and accomplished efficiently in an acceptable time.

Timing and spatial constraints arising from the circuit net list and placement prevent most of the devices from being active at the same time. Therefore, power grid simulation that considers all the circuit devices as simultaneously active is clearly unnecessary. Voltage drop and ground bounce may occur if there is a significant number of devices becoming active in a short period of time and drawing current from close regions of the power grid. We propose a technique to determine, within a time frame, how many devices become active on nearby regions of the power grid. The higher the number of devices in this situation, the greater the possibility of voltage drop and/or ground bounce effects be felt in the power grid (assuming the grid has a regular structure and that all devices take an equal amount of current) [7]. Combining timing and spatial information obtained in a traditional design flow it is possible to know when and which devices are active in order to generate a set of more realistic worst-case stimuli for grid verification.

II. A RELATED TRADITIONAL DESIGN FLOW

Simulation is the most commonly used method to validate the power grid. It enables one to verify if the power grid is suited for a given design, that is, if it is robust enough to deal with problems such as voltage drop and ground bounce. In Fig. 2 a simplified version of a standard design flow, with emphasis in power grid design and analysis, is presented. As can be seen in Fig. 2 a typical flow starts with a circuit description in VHDL or Verilog. This description is converted into a gate-level net list of a given technology library during logical synthesis. After synthesis, place & route of circuit cells is done. To ensure the circuit timing sign-off, static timing analysis (STA) is usually done afterwards. If STA fails, a new place & route should be performed. Then, power grid planning is done based on the knowledge of power distribution along the circuit [3]. However, this knowledge is, of course, rather limited. After the power grid design, a simulation (at electrical level) of the grid along with the “circuit” is performed. For that purpose, a RC extraction is done as well as the definition of power grid stimuli. This mainly consists on the definition of the circuit cells, which must be considered throughout the simulation, and their correspondent current waveforms.

Some of the simulation tools consider all the circuit devices as stimuli to the power grid. Others allow users to define which stimuli should be applied, i.e., which circuit cells are going to be considered during simulation. Most of the times this definition is based on user experience and knowledge. However, both options may deteriorate the quality and resulting accuracy of power grid simulation [8].

Figure 2. Traditional design flow (with emphasis on power grid

A critical region may be neglected if the user misses the combination of grid stimuli that will cause the worst voltage drop or ground bounce (a false negative). Results from a simulation obtained on the assumption that all cells need to be accounted for, may also identify invalid critical regions of the power grid that are supposedly affected by voltage drop or ground bounce (a false positive) [10]. This occurs because in normal working conditions all cells in the circuit cannot draw current from the power grid at the same time. Moreover, this type of simulation may also increase total runtime and memory requirements from simulators. After this simulation procedure, the designer will try to solve IR-drop problems, usually by placing decoupling capacitance inside those critical regions [14]. If those regions are non-critical, from a voltage drop and ground bounce point of view, the insertion of decoupling capacitance will only increase the overall static power consumption and it will be a waste of silicon area. This circuit changes can itself cause voltage drop and ground bounce to appear in other circuit regions.
III. CURRENT CHARACTERIZATION METHODOLOGY

For instantaneous Power Grid analysis, we analyzed cell peak current waveforms. Figure 3.1 shows transient waveform of inverter cell which was simulated at 250MHz. (VDD is power pin and VSS is ground pin) It has voltage waveform of primary input and primary output (VA, VY) of inverter. It also has current waveform in VDD and VSS port (IRVDD, IRVSS). The voltage waveform at VDD and VSS port is seen. (VVDD_INV1, VVSS_INV1). Note that current waveform at VDD and VSS are similar except one difference – transition direction. The current waveform at VDD when output is charging is same as current waveform at VSS when output is discharging and vice versa. This is true in this case for inverter but it can vary if the cell is not balanced properly. However in any case the amount of charge supplied/discharged will be constant since it is governed by load connected at output

Note here that the overall simulation time decreases when frequency increases for a same set of patterns. This is not a surprise as the load being charged and discharged is same during each transition for the same slew and for the same set of patterns. In case of CMOS gate, shape of current waveform remains same for very high frequencies (period ~ 3 times of 0-100% slew).

- The slew or transition time (used interchangeably) plays a big role for peak power determination of cells. When the slew decreases, the width of the current spike decreases with increase in peak. Figure 3.2 and Figure 3.3 shows the peak power variation for different input transition times. Note the variation of ~2x for inverter and ~1.5x for 2 input NAND gate.

Peak power varies while change in output load. The change is as expected since capacitance increase along with MOS resistance provides exponential voltage ramp up. Peak is largely dependent on MOS ON resistance as well as initial voltage. Figure 3.4 and Figure 3.5 shows the plot of variation for AND as well as OR gate. Note that the variation is ~1-3% across wide range of load.
For cell characterization, pattern dependency is not critical. This is expected as most of the circuits will be 1-2 level of logic where each pattern will activate/deactivate most of the transistors. However, soon when cells start becoming larger, some logic may not get activated during switching. In this case, it is important to choose useful patterns for cell current characterization [9].

- For cell characterization, transition direction matters for a given power supply. It means that output rise transition or fall transition are important to capture during characterization and use them appropriately during use. (Figure 3.1) In our case, we capture rise and fall transition together and use them for analysis, making proposed approach direction independent.

Figure 3.6 State Dependency on cell switching

1. Slew impacts the short circuit current of the device. For multi-stage block, slew impacts 1st stage the most and the overall current waveform is unaffected due to this change. The impact varies from lo to hi when the design stages are decreasing.

2. Glitches or hazardous transitions can contribute to peak current need of the circuit. Modeling glitches in non-SPICE analysis is not trivial. It is desired that glitches are reduced by robust design practices. In this work, it is assumed that there are no glitches in the design.

3. The temporal correlation between different inputs influences the characterization data a lot. This is due to simultaneous switching. We have used the least affecting combination i.e. 0 skew between multiple inputs in our analysis – this is worst case also. (Figure 3.6)

IV. ANALYSIS OF THE POWER GRID NETWORK MODELING

This section describes the Power Grid network building using cell characterization data. Power Grid offers resistance, capacitance as well as inductance to the switching logic. Figure 3.7 shows schematic of typical power grid. [15] The power & ground supply pins are modeled as ideal voltage sources. The methodology however vastly varies in terms of current source modeling and capacitance estimation [5, 11, 14, 3].

Figure 3.7 Power Grid Modeling

Once, the power grid is determined along with capacitance and current source distribution, it can be realized as matrix data structure and can be solved for computing voltages at desired nodes – specifically the nodes where cell components are connected as below.

\[ V \times Y = I \]

Where \( V \) is voltage value at each node, \( Y \) is admittance or resistance of PG segment, \( I \) is current that we have characterized.

\[ v(t) = Z \times i(t) \quad (Z = R - jW \text{ for power network}) \]

\[ V(w) = z(w) \times i(w) \]

In our work, we have computed resistances and capacitors based on technology data for 130nm node. A sample program was written to realize the mesh structure as shown in Figure 3.7 for VDD network and VSS was taken as ideal ground. This is not an issue since we can lump all the VSS network elements to VDD network. After determining Power Grid Current waveform, we solved the network through SPICE simulations [17].

A) Power Grid Current Waveform Modeling

Power Grid Current waveform modeling involves following steps:

1. Compute Toggle frequency for each of the instance in design
2. Transform the current data at the computed toggle frequency.
3. Compute the input arrival for each of the instance in design. This is done using Static Timing Analysis. Compute the shift required in current waveform with reference to clock edge. For simplicity, we have assumed 0 skew for clock network.
4. Hook up the current sources and solve the PG network.
5. Determine the PG model simulation time. These are explained further below.

A) Read the characterized data. Characterized data was transformed from time domain to frequency domain. The sampling is done at fixed frequency (much higher than common design frequency values) – 1000/75 ~ 13.33 GHz and [t, i(t)] are stored. 

\[ I(t) = i(0)d(0) + i(0+Ts)d(0+Ts) + i(0+2*Ts)d(0+2*Ts) + \ldots N \text{ Samples} \]

Where, 'Ts' is sampling frequency – in this case 13.33 GHz

\[ i(t) = i(n) \text{ when } t=n*Ts \text{ else 0. } \]

For computation efficiency N may be chosen as power of 2… N = 2 ** n (n is integer) Now, the Fourier transform of the samples have been performed:

\[ I[k] = |i[n]|^2 \]

B) Model the current waveform for each Boolean gate at computed toggle frequency.

- A compression factor (M) is defined to meet the targeted frequency of the cell under consideration.

\[ M = \frac{\text{targeted frequency}}{\text{cell characterized frequency (10MHz in this work)}} \]

- Transformation allows preserving base of the current transients. This would not have been possible in a time domain while we scale frequency. Hence, the need of frequency domain transformation.

- Current data is compressed by compression factor.

- When the data was transformed to frequency domain and the frequency spectrum was seen, the notable point was that we had a good chunk of lower frequency components -signifying the approximate triangles of SPICE waveform and most of the medium to high frequency components were zero -signifying the zero or low-leakage portion of the power waveform.

C) Attach the current waveform at a PG node where this cell’s power or ground pin is connected.

D) Compute the total simulation time

- Computing lowest common multiplier (LCM) is computationally intensive for most designs. Even if we do that, the generated simulation time is prohibitively high. The memory space also becomes high.

- In reality we are using a smaller number than that to ensure less simulation time and more realistic data. Instead we computed simulation time as below.

\[ T\text{stop} = (\text{minimum toggle frequency, max delay}) \]

\[ = \text{Time Period of minimum freq cell} + \text{maximum delay of all cell outputs} \]

\[ = 2000 \text{ ns (for minimum frequency as 1 MHz and 1000 ns as worst delay)} \]

E) Establishing temporal relationship

Do timing analysis and based on input arrival time, the current waveforms are shifted along time axis. The purpose behind timing analysis is to establish temporal correlation between various nodes of the design i.e. even though 2 or more nodes have same toggle frequency; this will not switch all instances in design simultaneously unless needed. In this work, we have chosen to work with toggle frequency and delay instead of timing window [18][19]. The reasons,

Not all circuit nodes switch in all the clock cycles. Average activity computation establishes relative amount of switching among various nodes. This is possible because activity estimation techniques consider circuit functionality. Average switching activity for most of nodes is believed at 20% of the controlling clock frequency. In certain solutions, the average switching activity for non clock signals is assumed to be 10% only.

- Timing window method uses classical path sensitization to identify the interval of switching. Inherent assumption of STA that all activity on a path should finish within 1 clock period (unless specified explicitly using multi-cycle path), the timing intervals for all nodes will lie within a clock period. This makes whole approach of pseudo dynamic simulation pessimistic.

During timing analysis, we collected 2 sets of data. One, sensitization edge of the node i.e. whether the node is rising or falling at that time and second, delay of the node from reference node. It can be seen that any frequency higher than 1 MHz will have at least some repetition in its current signature i.e. a node is switching at 50 MHz (20ns) will have 50 repetitions of its current signature in 1000 ns simulation. By changing the minimum frequency, we can change the simulation time considerably. For example, by changing minimum frequency to 50 MHz, we can ensure that all the current sources with less than 50 MHz do not contribute (or contributes an average
current) to dynamic V drop analysis and in that case maximum simulation time can become only 20 ns. In all our analysis we have assumed 1 MHz as minimum frequency [16]. Number of points in piece wise linear current waveform is based on the sampling resolution that we did as first step after reading characterized data. An increase or decrease in this frequency can change the accuracy trading some runtime. In our analysis, we have assumed 75 ps as sampling interval.

Clock network toggles all the time. Also many designs aim for smaller insertion delays as well as near zero skew. This makes clock network as one of the largest contributor of total current as well as peak current.

CONCLUSION

Analysis approaches proposed in this work helps in robust power grid analysis. Power Dissipation in cell based CMOS design discussed. A flow was proposed to do power estimation in various design stages that can improve the accuracy of estimation. The flow also helps user to make run time and accuracy tradeoff. The result from simulations shows that shape of the current waveform remains the same if the patterns used are same across different frequencies.

REFERENCE


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